ADHESION LAYER FOR Pt ON SiO_2

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a divisional of U.S. Application No. 10/408,339, filed April 7, 2003, the disclosure of which is incorporated herein.

BACKGROUND OF THE INVENTION

[0002] The present invention relates to integrated circuit (IC) memory devices and, more particularly, to the inclusion of one or more thin layers, such as Si, Al, IrO_2, or Al plus TiN, as an adhesion layer between a noble metal layer, such as Pt, and a silicon dioxide (SiO_2) layer to form the electrode for high-k dielectric Dynamic Random Access Memory (DRAM) and Ferroelectric Random Access Memory (FRAM) applications.

[0003] Capacitors with high dielectric constant (high-k) materials as the dielectric are increasingly used in high density devices. The high-k dielectrics used in DRAM devices are generally formed at a high temperature oxidation ambient, as are ferroelectric materials used in FRAM devices. To avoid oxidation of the electrodes at these high temperatures, noble metal electrodes are used with the dielectric. Platinum (Pt) electrodes are typically used for the high-k dielectric capacitors in DRAM devices and for FRAM devices because of its excellent oxidation resistance and high work function. However, Pt poorly adheres to silicon dioxide and results in peeling of the Pt at various process steps, such as during the formation of the capacitor and during the following Back End of Line (BEOL) processes. To prevent peeling, an intermediate adhesion layer may be added between the Pt and SiO_2 layers. Currently, the adhesion layers used include Ti, TaSiN or TiN.

[0004] Though these materials can improve the adhesion between the Pt and SiO_2 layers in the "as-deposited" state, roughening of the Pt surface or a local peeling has been observed after the subsequent annealing step which is typically at a

temperature of 500 to 580°C in an oxygen ambient. Further, when high-k dielectric and ferroelectric layers are deposited at temperatures below 500°C, the layers have degraded film quality with decreased capacitance, which degrades the performance of the device.

[0005] It is therefore desirable to provide an improved adhesion layer between the noble metal electrodes and the SiO_2 layers. It is also desirable to provide an adhesion layer that prevents the peeling of the noble metal electrodes of the capacitor structures.

SUMMARY OF THE INVENTION

[0006] The present invention provides one or more adhesion layers which prevent the Pt electrode from peeling from the SiO_2. Such layers include IrO_2, Si, Al, or Al plus TiN as the adhesion layer.

[0007] According to an aspect of the invention, in a semiconductor capacitor structure formed on a silicon dioxide (SiO_2) substrate and having a noble metal electrode, an adhesion layer is disposed between the electrode and the SiO_2 substrate. The adhesion layer is selected from a group consisting of silicon (Si), aluminum (Al), aluminum (Al) plus titanium nitride (TiN) and iridium oxide (IrO_2).

[0008] According to a further aspect of the invention, an adhesion layer is selected from a group consisting of Si, Al, Al plus TiN, and IrO_2 and is disposed between a noble metal layer and a silicon dioxide layer.

[0009] According to another aspect of the invention, a high dielectric constant (high-k) capacitor structure is fabricated. An adhesion layer is deposited on a SiO_2 substrate. The adhesion layer is selected from a group consisting of Si, Al, Al plus TiN, and IrO_2. A noble metal bottom electrode is deposited on the adhesion layer.

[0010] In accordance with this aspect of the invention, a high-k dielectric material is deposited on the bottom

electrode. A top electrode is deposited on the high-k dielectric layer, and the top electrode and the high-k dielectric are patterned. An insulation layer is deposited thereon, and vias are opened in the insulation layer. A metal pad layer is deposited in the vias and atop the insulation layer, and the metal pad layer is patterned.

[0011] According to a still further aspect of the invention, a 3-dimensional capacitor structure is fabricated. A silicon dioxide layer is deposited on a substrate, and vias are opened in the silicon dioxide layer. Polycrystalline silicon is deposited into the vias, and the polycrystalline silicon is planarized and recessed back to form poly plugs in the vias. A barrier layer is deposited in the vias, and the barrier layer is planarized. An adhesion layer is deposited atop the barrier layer and the SiO_2 layer. The adhesion layer is selected from a group consisting of Si, Al, Al plus TiN, and IrO_2. A noble metal bottom electrode is deposited on the adhesion layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] The foregoing and other objects, aspects and advantages will be better understood from the following detailed description of the invention with reference to the drawings in which:

[0013] Figure 1 is a graph illustrating x-ray diffraction analysis data and showing the stability of IrO_2 at temperatures of up to 750°C.

[0014] Figure 2 is a cross-sectional view showing a planar capacitor structure of a device according to an embodiment of the invention.

[0015] Figure 3 is a cross-sectional view showing a first three-dimensional capacitor structure of a device according to another embodiment of the invention.

[0016] Figure 4 is a cross-sectional view showing a second three-dimensional capacitor structure of a device according to

a further embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

[0017] The invention is directed to the use of one or more layers, such as IrO_2, Si and Al plus TiN, that improve adhesion between an electrode layer and a SiO_2 layer.

[0018] IrO_2, as an example, has a good adhesion to silicon oxide as can be predicted by its oxygen bonding nature. IrO_2 remains stable up to 750°C when exposed to an oxygen ambient, as shown in Figure 1. Further, polycrystalline IrO_2 is conductive and can serve as a part of the electrode.

[0019] Alternatively, thin Si or Al layers can form a uniform thin silicon oxide or aluminum oxide layer underneath a Pt electrode to improve the adhesion of Pt on SiO_2 layer without decreasing dielectric film quality on the Pt.

1. Table 1, Adhesion Test Results

Adhesion Layer and Thickness	Pt Thickness	Adhesion (Mpam1/2)
None	1000Å	Failed
TiN, CVD, 50Å	1000Å	<0.16
TaSiN, 250Å	2500Å	0.24
Ti, PVD, 50Å	1000Å	0.26
Al, 100Å	1000Å	0.23
Al, 100Å, +Ti, 200Å	1000Å	0.32
Poly Si, 50Å	1000Å	0.30

[0020] Table 1 shows the adhesion properties of various materials after exposure in an oxygen ambient at 640°C for five minutes. Samples with a known chemical vapor deposited (CVD) TiN adhesion layer could not be tested since its adhesion was less than 0.16. Samples with known Ti or TaSiN adhesion layers had improved adhesion over the CVD physical vapor deposition (PVD) but were not suitable because of

dielectric layer degradation on a Pt/Ti or TaSiN/SiO_2 structure. Better or at least comparable adhesion was obtained for samples with a polycrystalline Si, Al, or Al plus Ti adhesion layers of the invention.

[0021] To test the adhesion, a planar capacitor structure, such as is shown in Figure 2, was prepared by first depositing an adhesion layer 21 on a SiO_2 layer atop a substrate (not shown). The adhesion layer is preferably Si, Al, Al plus Ti or IrO_2. A Pt bottom electrode 23 is then deposited atop the adhesion layer 21. A high-k dielectric 24 is then deposited atop the adhesion layer, and a top electrode 25 (Pt) is deposited thereon. The high-k dielectric may be a (Ba,Sr)TiO_3 (BST) material. The top electrode 25 and the high-k dielectric 24 are then patterned and an insulation (SiO_2) layer 26 is thereafter deposited atop this structure. Vias are then opened in the SiO_2, and a Al or W a metal pad layer 27 is deposited in and on top of the vias and is then patterned.

[0022] Electrical testing results using the planar capacitor structure shown in Figure 2 show essentially no change in the capacitance of the dielectric layer when using a poly Si adhesion layer, as Table 2 shows.

Table 2, Electrical Test Results

Adhesion Layer	Capacitance (pF)
None	350-400
Poly Si, 50Å	350-400

[0023] The adhesion layers of the invention may be used in any integration scheme where adhesion of the electrode to the SiO_2 layer is of importance. Without limiting the scope of the invention, two examples using three-dimensional capacitor structures on devices for a DRAM application are now described.

[0024] Referring to Figure 3, a SiO_2 layer 31 is formed on a

device substrate (not shown). Vias are opened in the SiO_2 layer 31, and a polycrystalline Si layer 32 is deposited on top of the SiO_2 and into the vias. The polycrystalline Si is planarized to remove any material atop the SiO_2 layer, using a chemical mechanical polish (CMP) process, and the polysilicon is then recessed back, leaving poly plugs in the vias between the surface of the SiO_2 layer. Next, a barrier layer 33 is deposited atop the SiO_2 layer and the poly plugs, and the barrier layer is likewise subjected to a CMP process. An adhesion layer 34 is then deposited, and a Pt bottom electrode 35 is deposited atop the adhesion layer. If a conductive adhesion layer is used, such as IrO_2 the bottom electrode is deposited directly onto the adhesion layer. Alternatively, if a non-conductive adhesion layer is used, the part of the adhesion layer that is over the barrier layer is removed, and then the bottom electrode 35 is then deposited. Thereafter, the bottom electrode layer is patterned to form a three-dimensional structure (not shown). A high-k dielectric, such as BST, is then deposited and is covered with Pt top electrode layer to form the capacitor structure.

[0025] An alternative three-dimensional structure is shown in Figure 4. First, a SiO_2 layer 41 is deposited on a device substrate (not shown). Vias are then opened in the SiO_2 layer, and a polycrystalline Si layer 42 is formed in the vias and atop the SiO_2. The polycrystalline Si is then planarized using a CMP process and recessed back, thereby leaving poly plugs in the vias. Next, a barrier layer 43 is deposited and subjected to a CMP process. A SiO_2 layer 44 is deposited and then patterned to form a three-dimensional structure, and an adhesion layer 45 is deposited thereon. A bottom (Pt) electrode 46 is deposited directly on the adhesion layer when the adhesion layer is conductive, such as when IrO_2 is used. Alternatively, the adhesion layer is removed in the regions above the barrier layer 43 and the bottom electrode is

thereafter deposited. The top planar part of the bottom electrode 46 is then removed (not shown), and a high-k dielectric, such as BST, is deposited and covered with a Pt layer to form capacitors.

[0026] While the invention has been described in terms of preferred embodiments, those skilled in the art will recognize that the invention can be practiced with modification within the spirit and scope of the appended claims.